In the Specification

Please amend the specification of this application as follows:

Insert the following paragraph after page 20, line 6:

--Fig. 9 illustrates the portion of register file **76** of datapath A **68**. As shown in Fig. **9**, register file **76** receives up to 15 read register addresses and corresponding valid signals. Conditional 5 to 32 address decode **212** selects from the 32 data registers. The data from the data registers selected by conditional 5 to 32 address decode **212** is read from RF core **214** which reads the 32 bits from each accessed data register. This data is supplied to the requesting execution unit groups A, S, C, M, D and CR. In the register write operation, Fig. **9** shows receipt of the write addresses. The 5 to 32 address predecode **216** selects from the 32 data registers. Predication condition data from the instructions supplies predication predecode **218**. Write kill unit **220** compares the predication condition data with the contents of predication registers **222**. Write arbitration **224** is responsive a WRITE_VALID signal from write kill unit **220** to permit data write. Data write is prohibited upon the absence of the WRITE_VALID signal effectively nulling the instruction. Predicated operation is further described below. The output of write arbitration **224** selects the write registers for write to RF core **226**. The data for the register write comes from the execution unit groups A, S, C, M, D and CR. Data may also be written to predication registers **222**. Fig. **9** also illustrates a path for exchange of predication data with datapath B **70** used when the destination register and the predication register are in differing datapaths.--